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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,902	07/24/2003	Hideyuki Otake	OKI.556	1200

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,902	OTAKE, HIDEYUKI	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 06-13-05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response To Amendments/ Arguments

1. The indicated allowability of claims 1 – 21 is withdrawn in view of the newly discovered reference(s) to Segawa et al. (US Patent Number 5,523,721). Rejections based on the newly cited reference(s) follow. The prosecution of this case is re-opened.

DETAILED ACTION

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. US Patent Number 6,400, 300) Segawa et al. (US Patent Number 5,523,721).

4. Regarding claims 1, 3, 8, 10, 15, 17, Leung et al. discloses a digital-to-analog converting circuit (fig. 1) comprising: a first potential terminal (Vref) for supplying a first potential; a second potential terminal (ground) for supplying a second potential; an output node (Vout) for outputting an analog signal; a first resistor circuit (the resistors below Vref) having a plurality of first resistors connected in series between a first node and the output node through a plurality of first connecting points (fig. 1) ; a first switching circuit (80, fig. 1) having a plurality of first switches each of which is connected between the first potential terminal and one of the first connecting points and the first node (fig. 1) ; a second resistor circuit (the resistors at the sub DAC 18) having a plurality of second

resistors connected in series between a second node and the output node through a plurality of second connecting points (fig. 1) ; a second switching circuit (22, fig. 1) having a plurality of second switches; and a control circuit connected to the first and second switching circuits for controlling the first and second switches (80 and 22 are known to be a decoder to control the switching means). Leung et al. does not specifically discloses a system wherein a second switching circuit having a plurality of second switches each of which is connected between the second potential terminal and one of the second connecting points and the second node. However, Segawa et al., in a related field, discloses a system that comprises a second resistor string (60) and a second switch (70) of which each is connected between the second potential terminal (ground) and one of the second connecting points and the second node (fig. 6) [second node be the top node shown in fig. 6]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Leung et al.'s system with that of Segawa et al. in order to provide a digitally controlled variable gain circuit for outputting an analog output voltage.

5. Regarding claims 2, 9, 16, Leung et al. discloses a digital-to-analog converting circuit (fig. 1), wherein the first switching circuit (80) has a first switch connected between the first potential terminal and the output node (fig. 1)

6. Regarding claims 5, 12, 19, Leung et al. discloses a digital-to-analog converting circuit (fig. 1) wherein the control circuit includes a first decoder for controlling the first switches and a second decoder for controlling the second switches (80 and 22 are known to be a decoder to control the switching means) (see col. 10, lines 42 – 46).

7. Regarding claims 6, 13, 20, Leung et al. discloses a digital-to-analog converting circuit (fig. 1), wherein the first potential is a reference potential and the second potential is a ground potential (fig. 1).

8. Regarding claim 7, 14, 21, Leung et al. discloses a digital-to-analog converting circuit (fig. 1), further comprising an amplifier (26) connected to the output node for amplifying the analog signal.

9. Regarding claims 4, 11, 18, both Leung et al. and Segawa et al. disclose all the limitations as discussed above except the digital-to-analog converting circuit wherein the first switches are P-channel type MOS transistors and the second switches are N-channel type MOS transistors. However, P-MOS and N-MOS transistors are known to be an active device capable of switching components or elements in a circuitry. It is also known in the art that transistors are used as an alternative way to switch elements in a system. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the combination of Leung et al. and Sewaga's system would achieve the same end result as the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
June 23, 2005